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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,422	06/13/2006	Youri Ponomarev	NL03 1497 US1	6431

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EXAMINER	
WHALEN, DANIEL B	
ART UNIT	**PAPER NUMBER**
2829	

NOTIFICATION DATE	DELIVERY MODE
04/10/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/596,422	PONOMAREV, YOURI	
	Examiner	Art Unit	
	DANIEL WHALEN	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4 and 6-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2,4 and 6-8* is/are allowed.

6)☒ Claim(s) *9-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claims 9-10** are objected to because of the following informalities: claim 9 recites "a gate channel consisting of *a strained Si layer* manufactured by a method in accordance with claim 1." However, it appears that claim 1 does not manufacture or form the strained Si layer. Claim 1 merely discloses forming an amorphous Si layer, not the strained silicon Si layer. One skilled in the semiconductor art would easily understand that there is a difference between the amorphous Si layer and the strained Si layer. Appropriate correction is required.

For examining purpose, the strained Si layer is considered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 9-10** are rejected under 35 U.S.C. 102(b) as being anticipated by Shih et al. (US Pub 20030077882 A1; hereinafter "Shih").

4. **Regarding Claim 9-10**, Shih teaches MOSFET structure comprising source, drain and gate, wherein said gate comprises a gate channel consisting of a strained Si

layer; said strained Si layer being manufactured by a method in accordance with claim 1 (fig. 1-7); semiconductor device comprising at least one MOSFET structure in accordance with claim 9 (fig. 1-7).

It is noted that claims 9 and 10 are product-by-process claims and therefore are treated according to MPEP 2113. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. Since Shih teaches all the structure (e.g. MOSFET structure consisting of a strained Si layer as a gate channel) implied by a claimed method, the claimed method does not distinguish from the prior art.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claim 11-13** is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as in view of Xiang et al. (US Pub 2004/0087114 A1; hereinafter "Xiang").

Regarding Claim 11 and 13, Cohen teaches a method for forming a strained Si layer comprising:

formation of an epitaxial SiGe layer (110) on a monocrystalline Si surface (100) of a substrate, the substrate including a support layer (160) and a buried silicon dioxide layer (150), the monocrystalline Si surface laver residing on the buried silicon dioxide laver (fig. 1),

ion implantation (200) of said Si surface layer and said epitaxial SiGe layer to transform said Si surface layer into an amorphous Si layer (100') and a portion of said epitaxial SiGe layer into an amorphous SiGe layer (110'), a further portion of said epitaxial SiGe layer being a remaining monocrystalline SiGe layer (uppermost portion of SIGe layer in fig. 4), said amorphous Si layer, said amorphous SiGe layer and said remaining monocrystalline SiGe layer forming a layer stack on said buried silicon dioxide layer (fig. 5),

re-crystallizing said amorphous Si layer and said amorphous SiGe layer, said amorphous Si layer being transformed into a strained Si layer (600) and said amorphous SiGe layer being transformed into a re-grown crystalline SiGe layer (520) (fig. 5-6; col. 5, lines 32-46).

However, Cohen is silent as to disclosing patterning said layer stack and depositing of a silicon dioxide capping layer on the patterned layer stack. It is noted that recited claim above fails to require any specific orders. Xiang discloses patterning the layer stack for forming active parts of a MOSFET structure (see fig. 2a, 2b, and 2h; page 3, paragraph 26; also applies to **claim 13**); depositing of a silicon dioxide capping layer on the patterned layer stack (page 3, paragraph 26). Therefore, it would have been obvious to one of the ordinary skill in the art at the time of the invention to combine

the teaching of Cohen with that of Xiang so as to isolate the region to function as active region that comprises channel, source, and drain.

It is noted that one skilled in the art would understand that performing thermal oxidation would form the silicon dioxide layer on the patterned layer stack.

7. **Regarding Claim 12**, Cohen teaches further comprising removing the re-grown crystalline SiGe layer by etching (fig. 7).

Allowable Subject Matter

8. **Claims 1, 2, 4, and 6-8** are allowed.

Reasons for Allowance

9. The following is an examiner's statement of reasons for allowance:

Regarding Claim 1, the prior art of record, alone or in combination, and to the examiner's knowledge does not teach, disclose, suggest, or render obvious, at least to the skilled artisan, the instant invention regarding a method of making a strained Si layer, particularly characterized by the steps of fabricating the device in combination with a step of depositing a silicon dioxide capping layer on said remaining monocrystalline SiGe layer; and bonding the silicon dioxide capping layer to a silicon dioxide surface4 layer of a second substrate and thereafter removing said support layer

and said buried silicon dioxide layer by etching. Claims 2, 4, and 6-8, which depend from an independent claim 1, is allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

10. Applicant's arguments filed 01/28/2008 have been fully considered but they are not persuasive. In response to applicant's argument that the references fail to show certain features of applicant's invention, applicant's argument on page 6, particularly 3rd paragraph (emphasis added), it is noted that the features upon which applicant relies (i.e., patterning the stack when the Si layer is amorphous allows the Si layer to slip on the buried silicon dioxide layer during re-crystallization while at the same time being constrained by the re-grown SiGe layer) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL WHALEN whose telephone number is (571)270-3418. The examiner can normally be reached on Monday-Friday, 7:30am to 5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. W./
Examiner, Art Unit 2829

Daniel Whalen
4-3-8

/Ha T. Nguyen/

Supervisory Patent Examiner, Art Unit 2829